

Daozheng Xue

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✉ @Daozheng_Xue

Education

Aug 2023 – present

Shanghai Jiao Tong University.

B.S. in Computer Science, ACM Honors Class.

ACM Honors Class is an elite CS program in SJTU for students ranked in the top 2% with aspirations in research.

Research Interest

My research interests broadly span large language models, with a current focus on new architectures, diffusion language models, new training mechanisms.

Research Publications

- 1 Beiya Dai, Yuliang Liu, Daozheng Xue, Qipeng Guo, Kai Chen, Xinbing Wang, Bowen Zhou, and Zhouhan Lin. *Context-level Language Modeling by Learning Predictive Context Embeddings*. Under review at ICML 2026. 🔗 URL: <https://arxiv.org/abs/2510.20280>.

Research Experience

Shanghai Jiao Tong University

Research Intern at the SJTU LUMIA Lab, advised by Prof. Zhouhan Lin.

Contextlm: Hierarchical Models Interacting with High-level Abstract Concepts Jun. 2025 – Oct. 2025

Explored concept representations beyond the token level, aiming to design hierarchical architectures capable of extracting and utilizing high-level abstract concepts. (Under review at ICML 2026)

Dynamic chunking Contextlm

Nov. 2025 – present

Introduce the dynamic chunking mechanism for origin Contextlm by a simple prediction of future tokens, Improve the efficiency of computational resource allocation. (Planned submission to NeurIPS 2026)

Awards

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|-----------|---|------------------------|
| 2024-2025 | Zhiyuan Honor Scholarship | Zhiyuan Colledge, SJTU |
| | Awarded to top 2% students in SJTU annually | |
| | Academic Excellence Scholarship | SJTU |
| | Awarded to students with top academic performance in SJTU | |

Personal Projects

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|-----------|---|---|
| Mar. 2025 | Linear Crossformer | Course Project of Machine Learning |
| | An Incremental Try For Crossformer | |
| | Introduce the linear attention to enhance the efficiency and performance of Crossformer | |
| Feb. 2025 | MY Compiler, CPU and OS | Course Project of Compiler, Computer Architecture, Operating System |
| | compiler for Mx (a C-like educational programming language) to RISC-V backend | |
| | A RISC-V General Purpose CPU with Thomaslo architecture (Verilog). | |
| | An operating system on RISC-V platform finishing by RUST. | |

Skills

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|-------------|------------------------------------|
| Programming | C/C++, Python, Java, Verilog, Rust |
| Tools | Git, Docker, LaTeX, Markdown |